REMARKS

After entry of this amendment, claims 1-29 are pending. In the present Office Action, claims 1-11, 13-21, and 23-28 were rejected under 35 U.S.C. § 102(b) as being anticipated by Tran, U.S. Patent No. 6,016,533 ("Tran"). Claims 12 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran in view of Wickeraad et al., U.S. Patent No. 6,490,654 ("Wickeraad"). Applicants respectfully traverse these rejections and request reconsideration.

The Office Action requested that support be identified for any amendments to the claims. The amendment to reword "a set of storage locations" as "the set" is merely a slightly rewording for clarity, and thus the original independent claims themselves support the amendment. Additionally, see, e.g., Fig. 9 and specification page 27, lines 20-22 and page 28, lines 4-6. The insertion of "wherein each of the plurality of values comprises a plurality of bits associated with a corresponding cache line stored in the cache" finds support, e.g., in Fig. 9 and specification page 28, lines 18-23. The amendment to claims 2 and 14 is inherent in the original language of claims 2 and 14, and is also supported at, e.g., page 28, lines 6-10. The amendment to claim 10 is supported, e.g., at page 30, lines 8-15. New claim 29 is supported, e.g., at page 19, line 19-29.

Claims 1-29

Applicants respectfully submit that claims 1-29 recite combinations of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "the memory is configured to output a plurality of values from the set in response to the decoder selecting the set, wherein each of the plurality of values comprises a plurality of bits associated with a corresponding cache line stored in the cache …the circuit is configured to generate a way prediction for the cache responsive to the plurality of values [output from the set selected in the memory] and the first value [corresponding to the first address]".

Applicants respectfully submit that Tran does not anticipate the above highlighted features. Tran teaches way prediction for a data cache in which a plurality of storage

locations store way predictions [Tran, col. 3, lines 20-22], and way predictions are selected from the storage locations based on a first portion of the input address [Tran, col. 3, lines 22-24]. The decoder selects a subset of the memory locations in the cache based on decoding a second portion of the address and the way predictions [Tran, col. 3, lines 25-29]. It is important to note that these memory locations that are selected based on the way predictions and decoding the second portion of the address are not the locations storing the way predictions, but rather are the memory locations that store the cache lines themselves. In one embodiment, Tran's decoder selects a subset of the way predictions that were selected based on the first portion of the input address using the second portion of the input address [Tran, col. 3, lines 41-44].

Thus, to summarize, Tran selects way predictions based on a portion of an input address, and uses those way predictions and another portion of the input address to select a cache memory location from which to output data. Nowhere does Tran teach or suggest **generating a way prediction** for the cache responsive to a plurality of values output from a memory (and each of the plurality of values is associated with a cache line and is output from a set in the memory responsive to an indication of the first address) and further responsive to a first value that corresponds to the first address, as recited in claim 1.

That is, Tran stores way predictions and outputs them to select a cache memory location to output cache data. The stored values are the way predictions. Claim 1 recites storing values in a memory (where each value is associated with a corresponding cache line), outputting those values in response to an indication of the first address, and generating the way prediction for the cache using those values and a first value that corresponds to the first address. Each way prediction in Tran, by contrast, corresponds to a set of cache lines and predictions which way in the set will hit.

For example, in one embodiment, the circuit that generates the way prediction comprises comparators (e.g. claim 2 recites that the circuit comprises a plurality of comparators, wherein each comparator of the plurality of comparators is configured to

compare a respective one of the plurality of values to the first value, and wherein the circuit is configured to **generate the way prediction predicting a first way** of the cache for which the corresponding value of the plurality of values matches the first value as indicated by the plurality of comparators). The Office Action asserts that Tran anticipates claim 2, citing the comparison of tags to the address to detect a hit or a miss in the cache (see, e.g., Office Action page 3, last paragraph extending to page 4). However, Tran uses the tag comparisons to detect hit or miss in the cache. This does not anticipate using a plurality of comparators to generate a way prediction, as recited in claim 2 (in combination with the features of claim 1).

For at least the above stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 2-12 depend from claim 1 and recite additional combinations of features not taught or suggested in the cited art.

Claim 13 recites a combination of features including: "outputting a plurality of values from the set in a memory in response to the set being selected, wherein each of the plurality of values corresponds to a different way of the cache, wherein each of the plurality of values comprises a plurality of bits associated with a corresponding cache line stored in the cache; and generating a way prediction for the cache responsive to the plurality of values and a first value corresponding to the first address". The same teachings of Tran highlighted above with regard to claim 1 are alleged to teach the above highlighted features of claim 13. Applicants submit that Tran does not teach or suggest the above highlighted features of claim 13, either. Accordingly, claim 13 is patentable over the cited art. Claims 14-22 depend from claim 13 and recite additional combinations of features not taught or suggested in the cited art.

Claim 23 recites a combination of features including: "the memory is configured to output a plurality of values from the set in response to the decoder selecting the set, wherein each of the plurality of values comprises a plurality of bits associated with a corresponding cache line stored in the cache …the circuit is configured to generate a way prediction for the cache responsive to the plurality of values [output from the set selected

in the memory] and the first value [corresponding to the first address]". The same teachings of Tran highlighted above with regard to claim 1 are alleged to teach the above highlighted features of claim 23. Applicants submit that Tran does not teach or suggest the above highlighted features of claim 23, either. Accordingly, claim 23 is patentable over the cited art. Claims 24-29 depend from claim 23 and recite additional combinations of features not taught or suggested in the cited art.

Information Disclosure Statement (IDS)

The Office Action indicated that two patent references were not considered because the inventor names did not match those listed on the IDS: U.S. Patent No. 5,802,594 (listed as Wang et al., but should have been Wong et al.) and U.S. Patent No. 5,521,306 (listed as Tran, but the patent number has two transposed digits and should have been U.S. Patent No. 5,251,306). Applicants thank the Examiner for his careful review of the citations, and submit a supplement IDS herewith that corrects the citations.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-97500/LJM.

Respectfully submitted,

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